REMARKS

Entry of this amendment in this application, and its favorable reconsideration, are respectfully requested.

Claims 1 through 16 remain in this case. Claims 10 and 16 are amended.

The allowance of claims 4, 5, 7, 9, 11, 12, and 14 is noted.

Claim 10 is amended to correct a minor error of a typographical nature in its preamble. Entry of this amendment to claim 10 is respectfully requested.

Claim 16 was objected to because its preamble, as previously amended, recited that the claim was still dependent on claim 15, which of course was inconsistent with the remainder of its limitations in which the claim was intended to be placed in independent form. Claim 16 is amended to correct the error. Applicants submit that claim 16 is now in proper form.

The provisional obviousness-type double patenting rejection of claim 10 is noted. Upon allowance of either this case or the copending application S.N. 10/022,972 upon which the rejection is based, and assuming that the double patenting rejection is still appropriate (depending on the claims in the respective applications at that time), Applicants will then consider a terminal disclaimer to obviate the basis of the rejection.

Claims 1 through 3, 6, 8, 10, 13, and 15 were finally rejected under §102(b) as anticipated by the Guerra et al. reference[1].

As previously argued,[2] claim 1 requires the executing of a first program at source hardware operating according to a first instruction set architecture, and the executing of a second program at target hardware operating according to a second instruction set architecture.

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[1] Guerra et al., "Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification", *ACM* (June, 1999), pp. 964-69.
[2] In the Amendment of November 29, 2004.

Applicants maintain that claim 1 and its dependent claims are novel and patentably distinct over the Guerra et al. reference, specifically because the Guerra et al. reference fails to disclose these steps.

The Guerra et al. reference is directed solely to a simulation system for modeling and verifying software for a DSP.[3] It is clear from the tenor of Section 2 of the Guerra et al. reference that its method is applied in the modeling, and system simulation, of a particular DSP.[4] It is the results of this model that are analyzed, or compared against the results of other models, in performing the verification method disclosed in the Guerra et al. reference.[5] Examples of models compared in the Guerra et al. reference include an instruction set architecture (ISA) model against a gate/RTL model.[6]

But nowhere does the Guerra et al. reference disclose that its method is performed by source and target hardware that execute first and second programs, much less in a manner required by the collecting, determining, and indicating steps of the claim. Instead, the Guerra et al. reference discloses but a single hardware system ("a 296 MHz Sun Ultra2 with 2 Gigabytes of RAM"[7]) that runs both models. There is simply no disclosure whatsoever from the Guerra et al. reference of the executing of a first program at source hardware, and the executing of a second program at target hardware. Models are not hardware, they are instead software; as such, two distinct models are not two distinct hardware systems. In fact, considering that the Guerra et al. reference discloses only a simulation system[8], one could readily conclude that it fails to disclose any "target" hardware whatsoever.

For this reason, Applicants submit that the method of claim 1 is in fact novel over the Guerra et al. reference. Reconsideration of the final rejection of claims 1, through 3, 6, 8, and 13 is therefore respectfully requested.

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[3] Guerra et al., *supra*, page 964, Abstract.
[4] Guerra et al., *supra*, page 965-67, §2 (*i.e.*, §§2.1 through 2.4).
[5] *See* Guerra et al., *supra*, page 968, §4.1.
[6] Guerra et al., *supra*, page 964, right-hand column, ¶3.
[7] Guerra et al., *supra*, page 968, last paragraph.
[8] Guerra et al., *supra*, page 964, Abstract; page 965-67, §2 (*i.e.*, §§2.1 through 2.4).

Applicants further respectfully submit that there is no suggestion to modify the teachings of the Guerra et al. reference in such a manner as to reach the requirements of amended claim 1 and its dependent claims. As discussed above and as previously argued, the Guerra et al. reference is directed solely to full system simulation, on a single hardware system, of the operation of two different software circuit models. As a result, the techniques disclosed in the Guerra et al. reference are directed purely to such simulation, and are not applicable to hardware emulation and software verification carried out using two hardware systems, specifically source hardware and target hardware, and operating according to first and second instruction set architectures, respectively, as required by claim 1. Nor is there suggestion from the other prior art of record to so modify the teachings of the Guerra et al. reference.

Especially considering the important advantages of the invention of claim 1, including the automatic verification of a software application ported to another instruction set architecture system, by reporting discrepancies at or near the instruction at which the source and target versions vary,[9] Applicants therefore respectfully submit that claim 1 and its dependent claims are not only novel, but are also patentably distinct over the Guerra et al. reference and the other prior art of record in this case.

Independent claim 15 is directed to a digital system that includes a general purpose computer, first and second microprocessors, and first and second emulation hardware that control the operation of the first and second microprocessors, respectively, according to respective first and second instruction set architectures.

As previously argued, Applicants respectfully submit that claim 15 is novel over the Guerra et al. reference. Nowhere does the Guerra et al. reference disclose first and second microproceesors for executing application programs, nor does it disclose first and second emulation hardware that execute first and second programs, respectively, at the first microprocessor and second microprocessors. As discussed above relative to claim 1, the Guerra et al. reference is directed solely to a single hardware system ("a 296 MHz Sun Ultra2 with 2

[9] Specification, *supra*, page 4, lines 3 through 10; page 21, lines 15 through 25.

Gigabytes of RAM"[10]) that runs two models for verifying a DSP.[11] There are no first and second microprocessors disclosed by the reference. Nor are there are no first and second emulation hardware systems disclosed by the reference, much less such emulation hardware controlling the operation of first and second microprocessors according to first and second instruction set architectures, respectively. Again, models are not hardware, they are instead software, so two distinct software models are not two distinct hardware systems. Because the reference lacks disclosure of these specifically recited hardware resources of claim 15, the Guerra et al. reference necessarily fails to disclose the cooperative operation of a general purpose computer according as recited in the claim.

For this reason, Applicants submit that the final rejection of claim 15 under §102 is in error, and should be withdrawn.

Applicants further respectfully submit that claim 15 is patentably distinct over the Guerra et al. reference because there is no suggestion from the prior art to modify its teachings of the Guerra et al. reference in such a manner as to reach the requirements of the claim. As noted above, the reference is directed solely to full system simulation of the executing of an application program. There is no suggestion from the reference, nor from the other prior art of record, to apply even its disclosed techniques to a digital software verification system including first and second microprocessors and first and second emulation hardware, as required by claim 15, much less suggestion to then further modify the reference to operate a general purpose computer in the manner required by the claim. The important advantages provided by claim 15, as discussed above relative to claim 1, further support the patentability of the claim.

Applicants therefore respectfully submit that claim 15 is novel and patentably distinct over the Guerra et al. reference and the other prior art of record in this case.

Applicants maintain that claim 10 is also novel and patentably distinct over the Guerra et al. reference. As previously argued, Applicant submit that the Guerra et al. reference fails to

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[10] Guerra et al., *supra*, page 968, last paragraph.
[11] Guerra et al., *supra*, page 964, Abstract.

disclose or suggest the method steps recited by claim 10. Specifically, among others, Applicants respectfully submit that there is no disclosure in the Guerra et al. reference of the step of finding that a valid effective address is available based on a current effective address delay, nor is there disclosure of the computing of the effective address of an instruction if a valid effective address is not available, both steps required by claim 10. At most, the Guerra et al. reference discloses simply the delaying of interrupt handling if a conditional branch resides in the processor pipeline at the time of the interrupt.[12] There is no finding of whether a valid effective address for an instruction is available based on the current effective address delay, nor is there any computing of the effective address if a valid effective address is not available, all as required by claim 10. Applicants therefore submit that the final rejection of claim 10 as anticipated by the Guerra et al. reference is therefore in error and should be withdrawn.

And Applicants maintain that there is no suggestion from the Guerra et al. reference nor from the other prior art of record of the method of amended claim 10. There is simply no suggestion of the particular steps used to collect the first and second sets of events, as recited by claim 10. The greatly improved visibility into the operation of the application program being verified, as provided by the inventive method of claim 10, further supports the patentability of this claim.

Applicants therefore respectfully submit that claim 10 is and remains novel and patentably distinct over the prior art of record in this case.

Based on the above remarks, Applicants respectfully submit that entry of this amendment will place all claims in this case in condition for allowance. Alternatively, Applicants submit that this amendment will place the claims in this case in better condition for appeal, particularly relative to claims 10 and 16.

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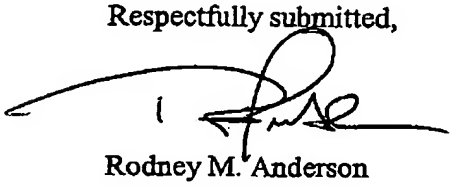
[12] Guerra et al., *supra*, page 966, right-hand column, lines 40 through 49.

Entry of this amendment in, and reconsideration of, this application are respectfully requested.

Respectfully submitted,



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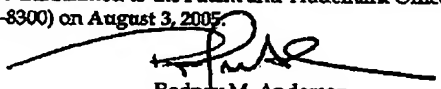

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